Remarks

Applicants thank the Examiner for his careful consideration of this application and for the helpful interview held on February 23, 2006. The contents of this interview are summarized in an attached Appendix. Reconsideration of this application is now respectfully requested in view of the amendments above and the following remarks, as well as the attached Affidavit.

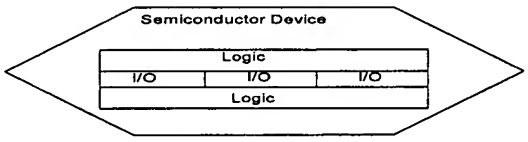
Claims 1 and 3-10, and 14-27 are now pending in the application, with Claims 1, 3, 16-18, and 21-24 being the independent claims. Claims 11-13 have been canceled without prejudice to pursue their subject matter in a future application. New Claims 20-27 have been added.

At pages 2-4, the Office Action rejects Claims 1, 3-5, and 16-18 under 35 U.S.C. § 103(a) as being unpatentable over Shenoy (U.S. Patent No. 5,994,766) in view of Sivilotti et al. (U.S. Patent No. 6,316,334). At pages 4-5, the Office Action rejects Claims 6-8 under 35 U.S.C. § 103(a) as being unpatentable over Shenoy and Sivilotti et al., further in view of IBM Technical Disclosure Bulletin 6/86, Vol. 29, No. 1, pp. 88-94 ("TDB") and Cox. At pages 5-6, the Office Action rejects Claims 9-15 under 35 U.S.C. § 103(a) as being unpatentable over Shenoy, Sivilotti et al. and TDB or Cox, and further in view of Hively. Finally, at pages 6-8, the Office Action rejects Claim 19 under 35 U.S.C. § 103(a) as being unpatentable over Shenoy and Sivilotti et al. in view of Hively and Cox. These rejections are respectfully traversed for at least the following reasons.

First, Applicants continue to maintain that the combination of Shenoy et al. and Sivilotti et al. is not technically possible and that it fails to teach or suggest all elements of the claimed invention. However, for the sake of brevity, Applicants have chosen not to rewrite their arguments to support this, but rather, the reader is referred to Applicants' Amendment filed on November 16, 2005.

Next, Applicants have elected to cancel, without prejudice, Claims 11-13, thus rendering moot their respective rejections.

Applicants have also elected to amend Claims 1, 3, and 16-18 (i.e., all remaining independent claims) to specify what is meant by an area I/O, per the discussion during the aforementioned interview. As discussed, "area I/O" is an art-recognized term, referring to an I/O placed within the body of a semiconductor device, as opposed to along its periphery (see, also, paragraph [0012] of the specification). Thus, it is inherent that at least one area I/O of a device containing area I/Os according to claimed embodiments of the invention will have logic adjacent to two opposite sides, as shown, for example, in the illustration below:



This illustration is intended to be a non-limiting example, and shows merely one possible configuration for area I/O.

As discussed during the interview, none of the cited prior art discloses or suggests the use of area I/O. On the contrary, for example, Shenoy et al., as discussed above, teaches that "I/O ports are disposed within I/O 'slots'" that are typically arranged in linear arrays "**along the periphery** of an integrated circuit device." Shenoy et al., col. 5, lines 7-12 and figures. It is also noted that Sivilotti et al., at col. 3, lines 18-28 and in Fig. 3, teaches the placement of I/O on the periphery of the disclosed device. I/O arranged in an array on the periphery of a device cannot have logic adjacent to two opposite sides because, for a given I/O, one side will face the outside of the device, and two sides will face other I/Os, thus leaving only one side to which logic may be adjacent. For at least this reason, it is respectfully submitted that Claims 1, 3-10, and 14-19 are allowable over the cited prior art.

Applicants further note the contemporaneously-submitted Affidavit of Mr. Zvi Or-Bach. In this Affidavit, Mr. Or-Bach notes that, to his knowledge, borderless/continuous arrays are not available from any commercial vendor of structured ASICs or gate arrays. As discussed in the Affidavit, a reason for this is that, prior to the present invention, no one, to Mr. Or-Bach's knowledge, was able to effectively solve the problem of I/O scalability. That is, without area I/Os, there are only peripheral I/Os, which leads to either insufficient I/O for small devices or very poor area efficiency for

larger devices. The use of area I/Os addresses this problem in that area I/Os may be embedded within the array, permitting the number of I/Os to increase proportionally with the needs posed by the size of the array. Hence, Applicants' invention has solved a heretofore unsolved problem and addresses a long-felt need, making viable a technology (the use of continuous/borderless logic arrays) whose use had been proposed in the past, but which had not been commercially viable.

Therefore, even if Shenoy and/or Sivilotti et al. and/or the other cited prior art were to teach or disclose all of the claimed subject matter (and Applicants do not agree that they do so), it would not have been obvious to one of ordinary skill in the art at the time the invention was made to create the claimed invention. For this further reason, it is respectfully submitted that Claims 1, 3-10, and 14-19 are allowable over the cited prior art.

Applicants have added new Claims 20-27. Claim 20 depends from Claim 1 and recites the placement of some area I/Os in spaced parallel lines. This is similar to the limitation found in original Claim 4, but depending from Claim 1. It is respectfully submitted that Claim 20 is allowable over the cited prior art for at least the same reasons for which Claim 1 is allowable.

Claims 21-24 are independent claims, each of which includes a recitation of the use of area I/O. For at least this reason, the above-mentioned arguments apply to these

claims, as well, and these claims, and Claims 25-27, which depend from Claim 24, are all allowable over the cited prior art.

It is noted that the limitations of these claims may all be found in the various claims as originally filed; however, these claims recite them in different combinations. These claims are thus supported at least by the originally filed claims, as well as by various portions of the present specification.

While Applicants do not necessarily concur with the Office Action's characterizations of the claims and/or the references with regard to other claimed features, Applicants choose not to discuss each such feature. Consequently, the lack of explicit discussion is not to be understood as indicating tacit agreement with such characterizations.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants, therefore, respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is hereby invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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APPENDIX:

APPLICANTS' SUMMARY OF

INTERVIEW OF

FEBRUARY 23, 2006

SUMMARY OF INTERVIEW OF FEBRUARY 23, 2006

Once again, Applicants thank the Examiner for the helpful interview held on February 23, 2006. The following represents Applicants' summary of what was discussed during the interview.

The interview on February 23, 2006 was attended by Examiner Tuan Quach, Mr. Zvi Or-Bach, a co-Applicant, and Dr. Jeffrey Gluck, Applicants' representative. The interview commenced with an introduction of Mr. Or-Bach to Exr. Quach and a discussion of Mr. Or-Bach's achievements, honors, and status within the field of endeavor of the present application.

The initial substantive discussion focused on arguments for non-obviousness of the claimed invention based on market-related considerations. In particular, Mr. Or-Bach pointed out that, to his knowledge, there has been no commercially-available continuous array (at the very least, not in the structured ASIC and/or gate array markets). Mr. Or-Bach discussed that use of such arrays has been suggested, but it has been impractical, and others have failed to make it commercially viable. A reason for this, said Mr. Or-Bach, is that the use of peripheral I/Os limits the scalability of the arrays due to the exponential growth in I/O requirements with increasing device area, as opposed to the only linear capability for growth in I/O capability using peripheral I/O. By introducing the use of area I/Os into the structure of continuous (borderless) arrays, Mr. Or-Bach discussed, a suitably scalable I/O arrangement may be obtained.

Mr. Or-Bach also noted that the primary references cited in the outstanding Office Action, Shenoy and Sivilotti et al., both teach devices using peripherally-placed I/Os. Therefore,

Mr. Or-Bach continued, the combination of area I/Os with continuous arrays, as shown, for example, in Figs. 36-38 of the present specification, is not obvious in view of the cited prior art. Exr. Quach suggested submitting an affidavit from Mr. Or-Bach, discussing these points.

However, Exr. Quach questioned the use of the term, "area I/O," and it was explained by Or-Bach and Gluck that this is an art-recognized term that refers to I/O that is found within the interior portion of a device, rather than on its periphery (as supported, e.g., by paragraph [0012] of Applicants specification). Exr. Quach suggested that embedding the definition within the (independent) claims would be helpful in limiting the interpretation of the claims. Or-Bach and Gluck agreed to include such a definition in Claims 1, 3, and 16-18 and to state that at least one claimed I/O is an area I/O.

Claims 11-13 were also discussed. It was noted that these claims are directed to a configurable I/O feature (which Applicants maintain is not found in the cited prior art), as opposed to the use of area I/O. Therefore, Or-Bach and Gluck decided that these claims would be canceled in the present application and would be pursued in a future application, so that the focus of the present claims would be on the use of area I/O with borderless arrays. Exr. Quach suggested importing the definition of "configurable I/O" into the claims when such a future application is filed. Or-Bach and Gluck agreed to consider doing so and would make a decision when the claims of such a new application are prepared.

Finally, the question of what is meant by a "logic array" was discussed. Mr. Or-Bach maintained that this term has an art-recognized meaning that includes a uniform structure and that no such structure is taught in the Shenoy reference.